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PATENT
5298-02502/PM98019CIN THE UNITED STATES PATENT AND TRADEMARK OFFICEIn re Application of:
Sethuraman et al.

Serial No. 09/779,123

Filed: February 7, 2001

For: PLANARIZED SEMICONDUCTOR
INTERCONNECT TOPOGRAPHY
AND METHOD FOR POLISHING A
METAL LAYER TO FORM
INTERCONNECTGroup Art Unit: 2823
Examiner: Lee, H.

Atty. Dkt. No. 5298-02502

I hereby certify that this correspondence is being transmitted via
facsimile or deposited with the U.S. Postal Service with sufficient
postage as First Class Mail in an envelope addressed to:
Commissioner for Patents, P.O. Box 1450, Alexandria, VA
22313, on the date indicated below.

February 16, 2004
Date

Kevin L. Dwyer

AMENDMENT: RESPONSE TO OFFICE ACTION DATED NOVEMBER 14, 2003Mail Stop: Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir/ Madam:

This paper is submitted in response to the Office Action mailed November 14, 2003 to further
highlight reasons why the application is in condition for allowance.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 6 of this paper.